

# AN10952

## SSL2103 flexible, mains-dimmable LED driver

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Application note

### Document information

Info	Content
<b>Keywords</b>	LED, flexible LED driver, dimming, mains dimmable, LED lighting, LED lamp, SMPS, SSL2103, external power switch, flyback, power factor
<b>Abstract</b>	This application note describes how to design a mains dimmable LED driver using the NXP SSL2103 flexible LED Driver IC in flyback mode. It includes a description of how mains dimmer compatibility is achieved



## Revision history

Rev	Date	Description
v. 1	20101224	first issue

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## 1. Introduction

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Light Emitting Diodes (LED's) have been used in electronic systems for many years, primarily as indicator lights on electronic devices. Recent advances, in terms of brightness and available colors, mean that LEDs can now be used in a wide range of applications, from fun lighting in cell phones and media players to replacing conventional light sources in commercial and domestic lighting applications.

The key enablers driving the expansion of LED lighting, are the availability of high brightness LEDs and intelligent LED controllers. Product designers involved with incorporating high brightness LEDs, face many challenges. Amongst these challenges are thermal management, driver scheme/topology and existing infrastructure.

To replace an existing dimmable incandescent or halogen light source, an electronic lamp driver system must be implemented that can operate with the existing dimmer switch whilst replicating the dimming behavior of the existing light source. The SSL2103 offers extensive possibilities to assure stable operation with all current dimmers. With the SSL2103, full flexibility is offered for bleeder circuitry implementation. This allows the designer to optimize the application efficiency while keeping a high level of dimmer compatibility.

The SSL2103 provides a control output for an external power switch to extend its application reach towards a higher power domain.

Summarizing, the SSL2103 enables the lamp/module designer to produce an LED driver that:

- can drive any power
- has optimal dimmer compatibility
- is very flexible, cost and size effective, whilst benefiting from optimal thermal trade-off.

## 2. LED properties

LEDs need a completely different type of driver, to the type used with incandescent or halogen lamps. Incandescent lamps act as resistive loads with self-stabilizing properties whereas LEDs require a current source. The amount of light generated by an LED is approximately proportional to the current flowing through the device. The voltage drop across the device increases with current but decreases with temperature. In this respect, LEDs behave like diodes. However, the voltage drop during operation (the forward voltage or  $V_F$ ) is greater (see [Figure 1](#)). This voltage drop is related to the amount of energy (eV) generated when an electron is converted into a photon. The amount of energy generated is directly related to the color of the light. Additionally,  $V_F$  can vary greatly between batches due to production spread.

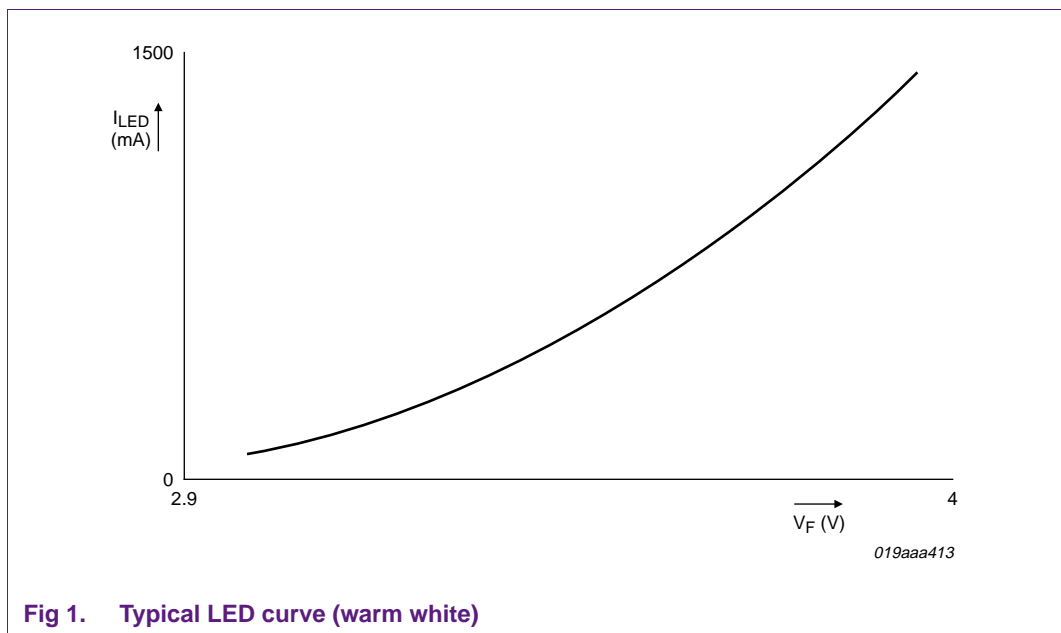


Fig 1. Typical LED curve (warm white)

### 2.1 Serial/parallel configuration

In most applications where LEDs replace existing lamps, multiple units need to be connected to the driver since a single LED would not generate enough light. The LEDs can be connected in either series or parallel.

If the LEDs are connected in series, the total voltage across the LED chain will be equal to the sum of the forward voltages (the current will be the same in all the LEDs).

If LEDs are connected in parallel, the current is distributed among the branches. However, because the forward voltage of an LED tends to fall as the temperature rises, this configuration is intrinsically unstable. As the temperature rises, more and more of the current generated will flow through the branches with the lower forward voltages. These branches will become brighter while the branches with the higher forward voltages become darker.

One reason for persisting with the parallel configuration (or a series-parallel combination), is that it allows a large number of LEDs to be combined on a safe supply voltage. An unacceptably high voltage might be needed to achieve the same degree of brightness with a series configuration.

The parallel configuration also offers the advantage of redundancy. If a single LED or connection in a series-connected LED chain fails, resulting in an open circuit, the light will extinguish in all the LEDs in the chain. This would not happen if the LEDs were connected in parallel. With a parallel configuration, it is recommended that current regulation is added at each branch to prevent thermal runaway and the unequal distribution of current and light.

In general, power converters operate at optimal efficiency when the difference between output and input voltages is minimized. With mains powered drivers and LEDs, optimizing this aspect will generate higher output voltages allowing more LEDs to be connected in series.

### 3. Flyback converter basics

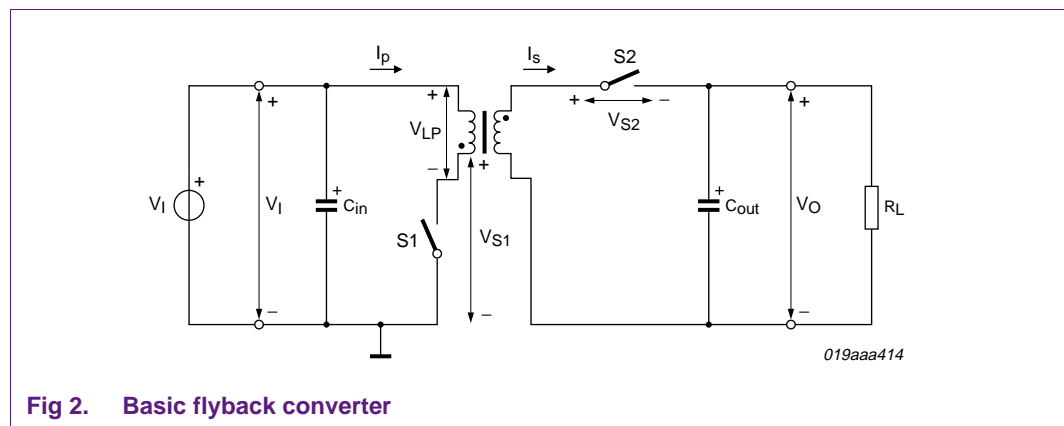
**Remark:** All components referred to in the text can be located on [Figure 9 “Typical flyback application using the SSL2103”](#) and switches can be found on [Figure 2 “Basic flyback converter”](#) and [Figure 3 “Flyback equivalent circuits and waveforms \(DCM mode\)”](#).

In many applications, isolation from the mains is necessary for safety reasons. The flyback converter provides this isolation. It is also less expensive and simpler to implement than a push-pull or a forward converter, since it only requires a single inductive element and a switch.

[Figure 2](#) is a simplified application diagram of an isolated flyback converter, connected to a supply and a load. The polarities of some relevant voltages and currents are included in this diagram. To help in understanding the application,  $V_I$  and  $V_O$  should be considered to be DC. In a practical applications, a MOSFET or bipolar transistor would replace switch S1 whilst a diode would replace S2.

The state of the switches determines the operation of the circuit. Two switches allow four possible operating states (see [Table 1](#)):

- States 1 and 2 - alternating primary and secondary conduction states
- State 3 - no primary or secondary conduction
- State 4 - both switches closed (must be avoided)



**Fig 2. Basic flyback converter**

**Table 1. Flyback converter operating modes**

State	S1	S2	Duration
1	closed	open	$\delta 1T$
2	open	closed	$\delta 2T$
3	open	open	$\delta 3T$
4	closed	closed	NA

Initially, switch S1 is closed (for  $\delta 1T$ ) and a current starts to flow in the primary winding of the transformer (state 1), rising linearly. Then S1 is opened and S2 is closed (for  $\delta 2T$ ) and the energy stored in the secondary winding of the transformer causes a current to flow in the load (state 2), which falls linearly as the energy is dissipated. The peak value of the load current is equal to the transformer primary-to-secondary turns ratio ( $n = N_p/N_s$ ) multiplied by the primary peak current at the instant S1 is opened. While S2 is conducting,

the output voltage is reflected in the primary side of the transformer. State 3 occurs when the secondary current falls to zero while S1 remains open (for  $\delta 3T$ ). Primary and secondary currents are both zero.

This mode of operation where the primary conducts for  $\delta 1T$  (the primary stroke), the secondary conducts for  $\delta 2T$  (the secondary stroke) and then conduction is halted for  $\delta 3T$ , is called Discontinuous Conduction Mode (DCM). If a new cycle begins as soon as the secondary current falls to zero ( $\delta 3T = 0$ ), the converter is operating in Boundary Conduction Mode (BCM).

[Figure 3](#) shows the equivalent circuit diagrams for the three valid states when a converter is operating in DCM mode. Simplified waveforms for one complete switching cycle are also shown.

More detailed discussions of the operation of flyback converters can be found in electronic engineering reference books.

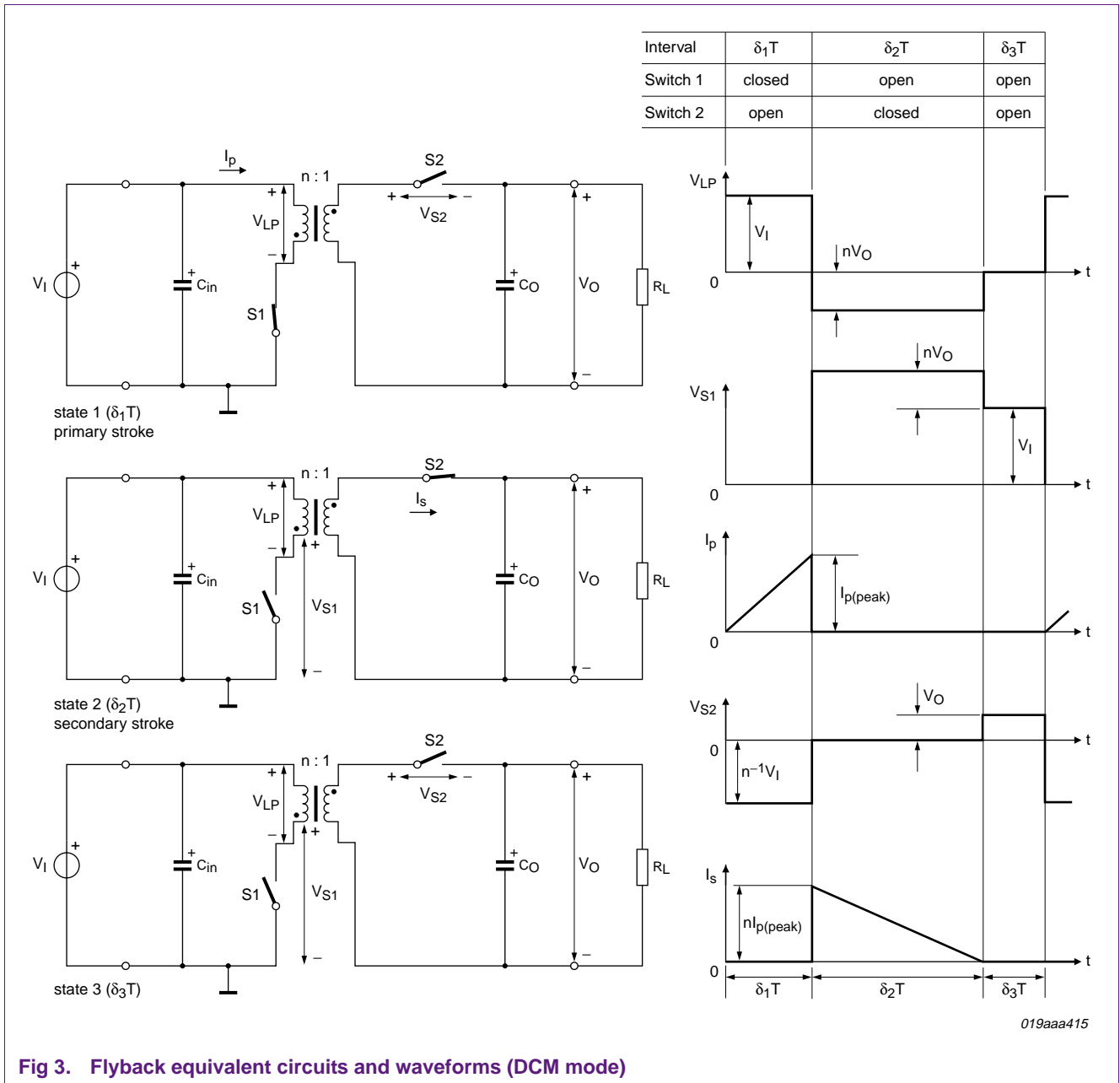


Fig 3. Flyback equivalent circuits and waveforms (DCM mode)



## 4. Mains dimming

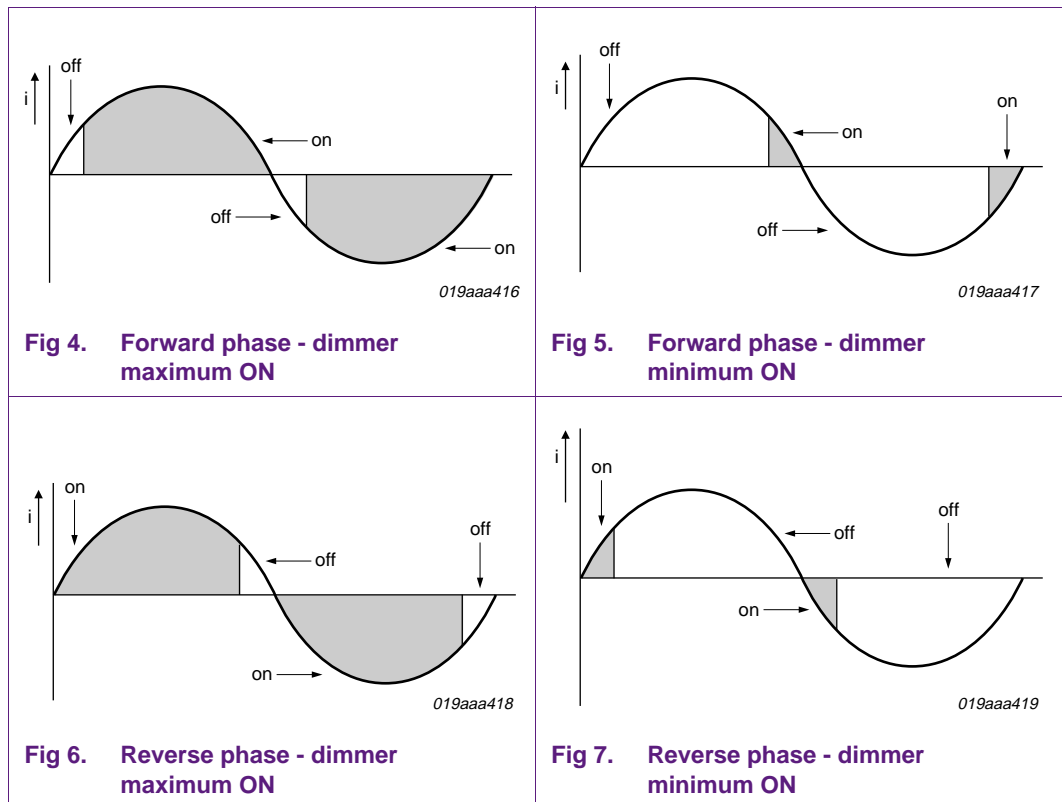
Standard industrial and household dimmers were designed for use with incandescent lamps. Some of the more advanced types can be used with transformers connected to halogen lamps. LED-specific mains dimmers are still rare.

The costs of buying and installing a dedicated dimmer, can easily surpass that of the light source itself. So an LED system that will work with the existing dimming infrastructure, will open up this market segment. Because existing dimmers were designed for use with incandescent lamps (which approximate resistive loads dissipating between 20 Ω and 500 Ω), some additional circuitry will be needed to allow them to be used in an LED system. There is no standard for incandescent dimmers, which in practice leads to a large spread in performance and parameter values.

The SSL2103 offers extensive possibilities to assure stable operation with all available current dimmers.

### 4.1 Dimmer switch classification

Dimmer switches work by turning off power to the lighting circuit during part of the supply cycle. By rapidly turning the light circuit on and off (twice for each cycle of the supply voltage, or 100 to 120 times per second), the total energy delivered to the lighting element is reduced. The longer the power is off during each cycle, the dimmer the light will be. The thermal persistence of the filament smooths out the pulses, ensuring imperceptible flickering due to the rapid switching.



Dimmers can be divided into two operational categories: positive angle/forward phase operation, also known leading edge dimming, and negative angle/reverse phase operation, or trailing edge dimming.

Forward phase dimmers work by varying the switch ON point of the supply current to a lighting circuit. They detect the start (zero-crossing point) of each half-cycle of the supply voltage, and then wait for a predetermined period before switching on the current (see [Figure 4](#) and [Figure 5](#)).

Reverse phase dimmers vary the switch OFF point, cutting off the supply current to the lighting circuit at predetermined intervals (see [Figure 6](#) and [Figure 7](#)).

Two switching methods can be distinguished: triac dimming and transistor dimming. Triac switching is always used with forward phase dimmers. Transistor switching can be used with forward and reverse phase dimmers. Transistor dimmers have the advantage of being able to switch capacitive loads, but most existing dimmers are still triac based.

## 4.2 Triac dimmer

A triac is a bidirectional gated switching device with distinct latching properties. A number of conditions must be met to ensure reliable latching and to maintain current flow once the device has been latched:

- When the triac is triggered, the voltage across the device must be sufficient to enable the minimum latch current to flow.  $I_L$  is the minimum current needed to hold the component in the conducting state after the trigger (or gate) current has been removed.  $I_L$  must flow for long enough (the firing time) to completely latch the device.
- Once the device has been latched, a continuous current must flow through the device in one direction. This is the hold current,  $I_H$ . If the polarity of  $I_H$  changes (i.e. at a zero cross point), the triac will switch off.
- A triac is not a fully symmetrical device - the values of the above parameters depend on the direction of current flow and on temperature. A timing circuit inside the dimmer, usually consisting of a resistor/capacitor combination, must be reset at zero crossing (the capacitor must be fully discharged).

If the above stable dimmer operation conditions are not met, problems may arise that can lead to unstable operation. LED systems without oversized buffering are unforgiving, because they respond a lot faster to changes in power dissipation than incandescent lamps do. Even small variations in light output in the response frequency of the human eye (200 Hz to 120 Hz) can cause flickering and be disturbing. So the switching frequency should not be allowed to fall below 200 Hz. It should be noted that the human eye is more susceptible to variations in color than brightness.

## 4.3 Transistor dimmer

A transistor dimmer uses a rectifier bridge in combination with a switching device, such as a MOSFET or bipolar transistor, to switch the main current. It contains additional circuitry to drive these devices, and this circuitry needs to be powered. The power is tapped from the switch while it is open, and stored in a capacitor. Though the energy dissipated in the dimmer electronics is not substantial, the current drawn over the switch can be a lot greater than the current required for a passive timing circuit.

## 5. Functional description

The SSL2103 is a Multi-Chip Module (MCM) in an SO14 package and has the same core controller functions as the SSL2101 and SSL2102.

The main differences between the SSL2103 with respect to the SSL2101 and SSL2102 are:

- The SSL2103 has a control output for an external power switch to drive any power. This is to extend the application reach towards a higher power domain.
- Drive outputs for real current source bleeder control are available and are preferred to resistive bleeder switching as they provide better dimmer compatibility.

Further advantages over existing solutions, which are the same as the SSL2101 and SSL2102, (see also [Figure 8](#)):

- Valley detection - this feature reduces converter losses, because the switch is closed at the optimal time.
- Smart bleeder operation - the IC senses when bleeder action is not required (e.g. the LED chain provides sufficient load). This reduces power dissipation and increases system efficiency.
- Enhanced thermal lead frame - this can increase the lifetime of the IC and enable it to operate at higher ambient temperatures. For retrofit solutions, the lifetime of electronics at elevated temperatures can be a critical parameter.
- Dimming by duty factor control and by converter frequency - this allows the designer more freedom when defining parameter values. More accurate control of low dim levels can be achieved, and audible transformer noise eliminated, by adjusting the parameters controlling both dimming systems.
- Logarithmic dimming correction - this enables the dimming behavior of the LEDs to replicate that of an incandescent or halogen lamp.
- Built-in thermal protection, overcurrent protection, short-winding detection and maximum duty factor limiting - these features ensure the reliable operation of the IC with minimum failures, even when operating outside specifications.

Further details and full specifications can be found in the SSL2103 data sheet (see [Ref. 1](#)).

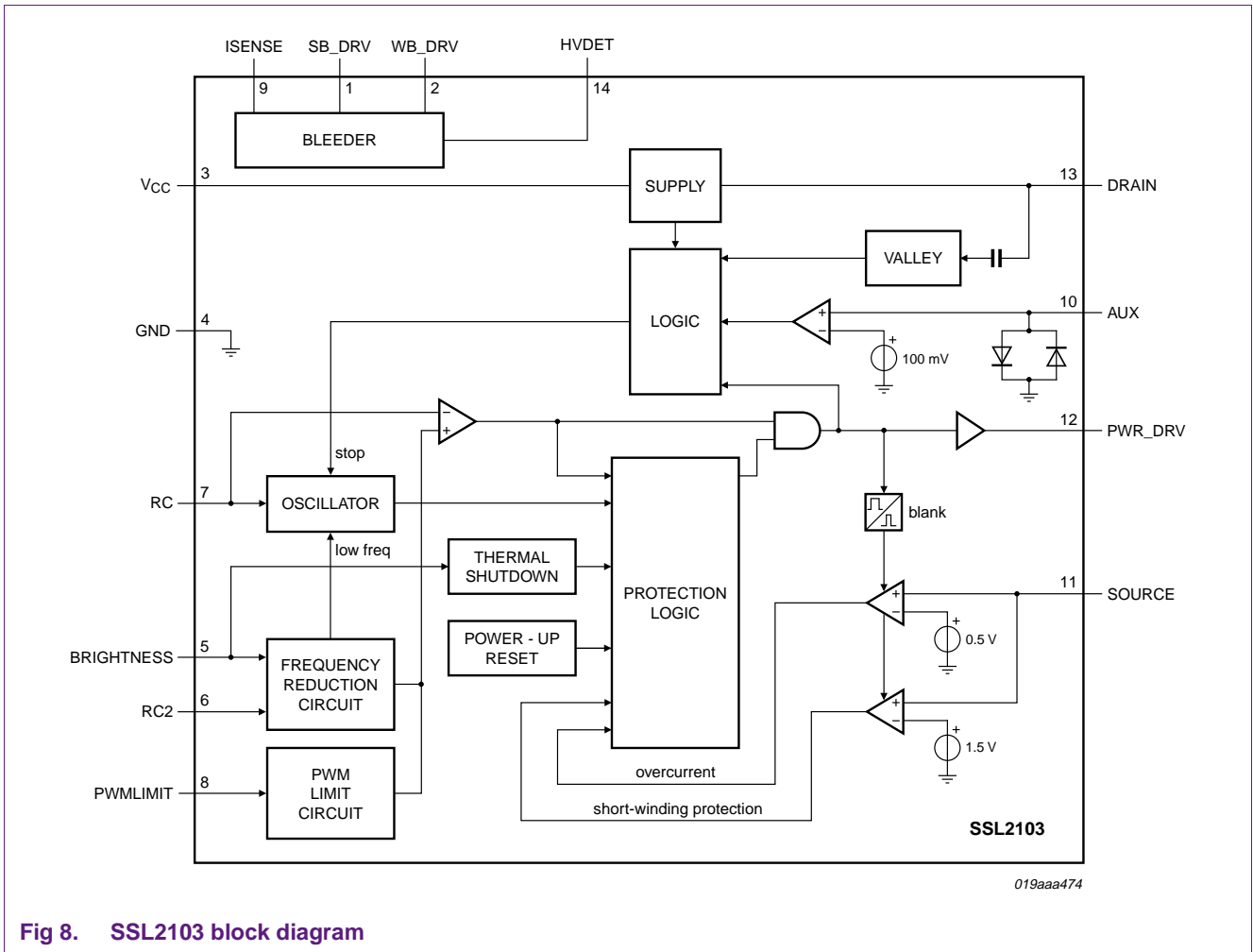


Fig 8. SSL2103 block diagram

## 6. Step-by-step design procedure

**Remark:** All components referred to in the text can be located on [Figure 9 “Typical flyback application using the SSL2103”](#) and switches can be found on [Figure 2 “Basic flyback converter”](#) and [Figure 3 “Flyback equivalent circuits and waveforms \(DCM mode\)”](#).

This sections provides a step-by-step guide to designing a basic flyback converter application incorporating the SSL2103. It should be noted that the derivation of the formulas applied is beyond the scope of this application note. Where values used in formulas are application specific, reasonable estimates have been made. Recommended component values were achieved through extensive testing with a range of commercially available dimmers.

### 6.1 Basic configuration

A circuit for a typical flyback application driving a single LED chain is shown in [Figure 9](#). The mains voltage is rectified, buffered and filtered in the input section and connected to the primary winding of the transformer. In the output section, the transferred energy is stored in a capacitor (C5) and filtered (L3) before driving the LED chain. A clamp is added across the primary winding of the transformer to prevent a high voltage overshoot on the DRAIN pin of the SSL2103, at the moment the external power MOS transistor is switched off. A dimming detection circuit divides and filters the mains rectified voltage to provide input for the generation of the dimming curve.

The following functional blocks can be identified in the SSL2103 application and they will be discussed separately (refer to [Figure 9](#)):

1. LED output current circuit
2. Oscillator
3. External power switch
4. Snubber
5.  $V_{CC}$  generation
6. A/B bleeder settings
7. Dimming detection
8. Mains buffer
9. Input circuit

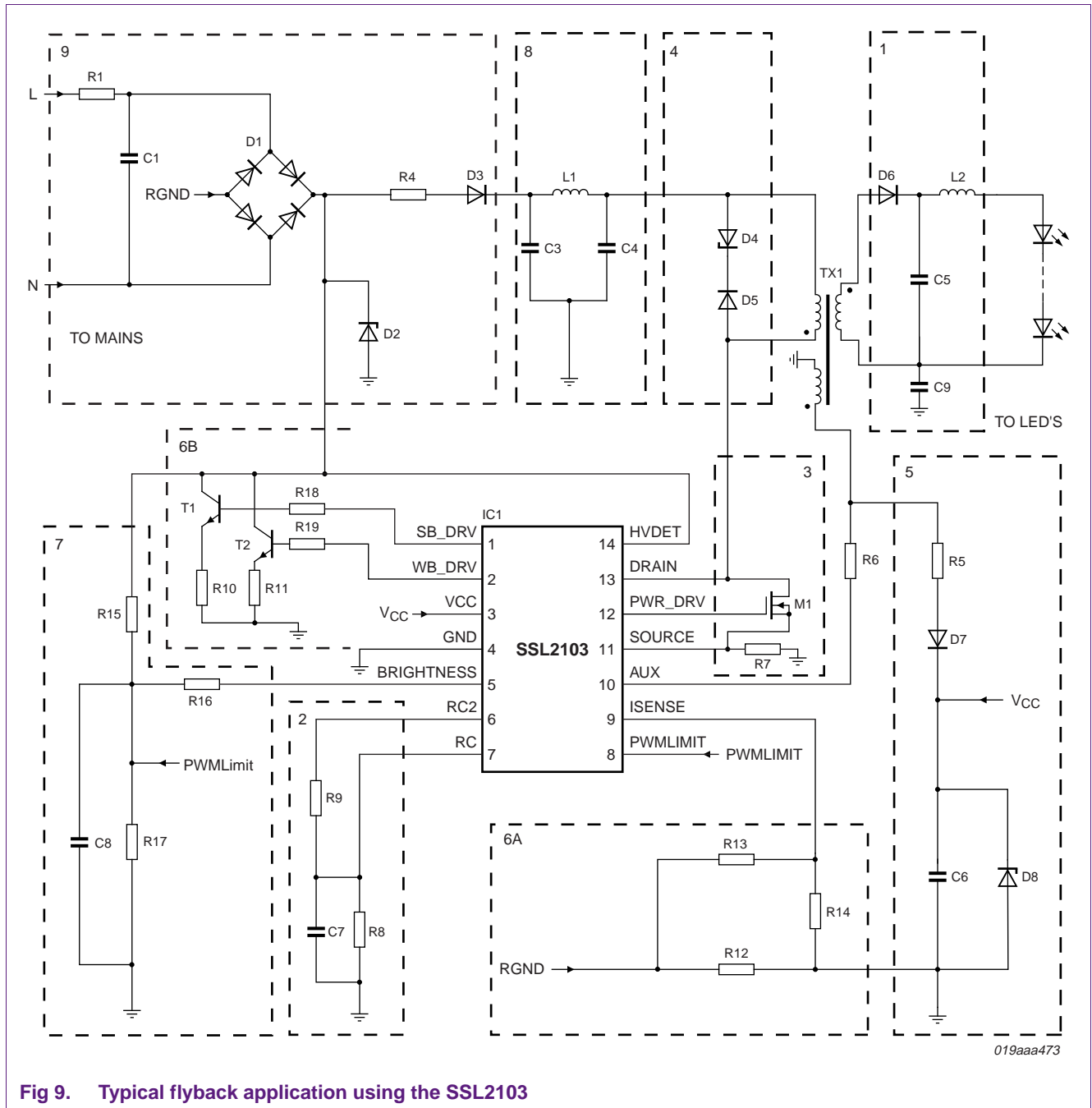


Fig 9. Typical flyback application using the SSL2103

## 6.2 LED output current circuit

The values of components in the output circuit will depend on the number of LEDs in the chain, the voltage across the chain and current through the chain. The current will have a ripple and the size of this ripple will dictate the size of the buffer capacitor (C5). The size of the buffer capacitor can be calculated from [Equation 1](#):

$$C5 = \frac{I_{LED}}{\Delta I} \times \frac{I}{f_{conv(nom)} \times R} \quad (1)$$

where:

$I_{LED}$  = LED current

$\Delta I$  = change in LED current

$f_{conv(nom)}$  = nominal converter frequency

R = series resistance of LED chain

In the design example ([Figure 9](#)):

- It is assumed there are 10 LEDs in series at 350 mA with a forward voltage ( $V_F$ ) of 3.5 V, a current ripple of 10 % and a nominal converter working frequency of 100 kHz.
- The voltage across the LED chain will be  $10 \times 3.5 \text{ V} = 35 \text{ V}$ . Assuming that each LED has a differential resistance of  $0.5 \Omega$  at 350 mA, the resistance of the LED chain will be  $10 \times 0.5 \Omega = 5 \Omega$ . which gives a buffer capacitor size of:

$$C5 = 10 \times \frac{I}{100000 \times 5} = 20 \mu F \quad (2)$$

When using an electrolytic capacitor for C5, it is recommended that a low ESR ceramic or foil capacitor be connected in parallel to improve EMC filtering and reduce dissipation. This capacitor should be mounted closer to D6 than the electrolytic capacitor, C5.

The output coil (L3) filters the high frequency signals from the converter. The size of this coil depends of the EMC norm to be applied on the final product and on the construction, grounding and screening. As a guideline, the cut-off frequency of the LR filter (consisting of the inductance of L3 and the resistance of the LED chain) can be chosen to be  $\frac{1}{20}$  th of the converter frequency. The coil value can be calculated using [Equation 3](#):

$$L3 = \frac{20 \times R}{2 \times \pi \times f_{conv(nom)}} \quad (3)$$

In the following example this will give an output coil value of:

$$L3 = 20 \times \frac{5}{2 \times \pi \times 100000} = 160 \mu H \quad (4)$$

Diode D6 must meet the following selection criteria:

- be able to withstand the peak current
- be able to withstand the maximum reverse voltage
- have a low voltage drop in forward mode
- have a low capacitance value in reverse mode

The peak diode current through D6 is determined by the secondary stroke time ( $\delta 2T$ ) and the LED current.

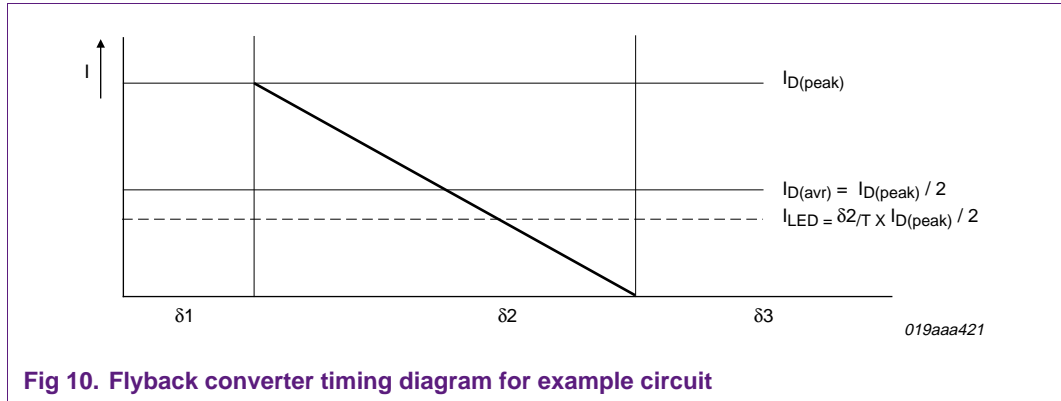


Fig 10. Flyback converter timing diagram for example circuit

The peak reverse voltage across D6 is determined by the primary-to-secondary turns ratio of the transformer and the maximum buffer voltage (the voltage across C3 and C4 in the mains buffer; see Figure 9). A margin must be applied here to allow for oscillation effects.

$$V_{rev(peak)} = \frac{V_{buff(max)}}{n} + V_O + V_{osc} \tag{5}$$

where:

- $V_{rev(peak)}$  = peak reverse voltage across diode
- $V_{buff(max)}$  = maximum voltage across capacitors in buffer circuit
- $n$  = transformer primary-to-secondary turns ratio
- $V_{osc}$  = margin applied for oscillation effects
- $V_O$  = Output voltage

D6 can be either a Schottky diode with a  $V_F$  of between 0.15 V and 0.4 V or a silicium diode with a  $V_F$  of around 0.7 V. Note, however, that Schottky diodes have a relatively low maximum reverse voltage. A suitable Schottky diode may not be available for a given application. One of the main parameters determining reverse capacitance is junction size, which is in turn related to maximum current over sizing of D6, which results in unnecessary losses.

C9 is connected between ground and the secondary circuit to counter capacitive coupling between primary, auxiliary and secondary windings. To be effective, the value of this capacitor should be much greater than the value of the capacitive coupling. As a general guide, a factor of 20 is recommended. So if  $C_{coup} = 100$  pF, C9 should be  $> 2$  nF.

If safety isolation is needed, this capacitor should be able to withstand the applied voltages as specified in EN132400 (type Yn).

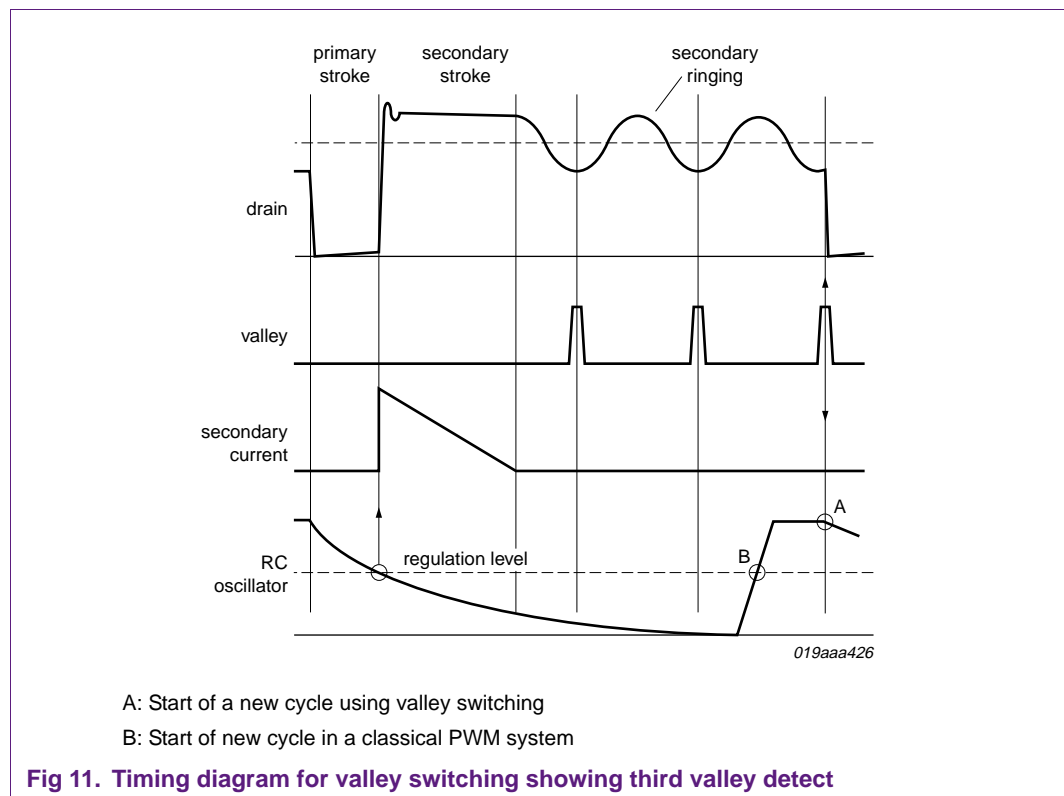


### 6.3 Oscillator components

The maximum converter and oscillator frequencies are determined by the primary inductance and the transformer input power (see [Section 7](#)). The transformer input power is the sum of the power dissipated in the output circuit, in the auxiliary circuit and the transformer losses. The corresponding formula that gives this relation is stated below:

$$L_p = \frac{2 \times P_{input}}{I_p^2 \times f_{conv}} \tag{6}$$

After the secondary stroke, the drain voltage oscillates at a ringing frequency,  $f_{ring}$ . The oscillator waits until it has detected a low drain voltage (a valley) before initiating a new primary stroke. The oscillator frequency is selected to achieve maximum efficiency and guarantee first valley detection (the first valley occurs after  $\frac{1}{2}$  of the period of  $f_{ring}$ ). The oscillator frequency can then be lowered using the brightness input for dimming. As the oscillator frequency is lowered, valley detection will be triggered at the second, third, fourth valleys, etc. thereby gradually increasing the off time ( $\delta 3T$ ).



It can be seen from [Equation 6](#), that there is a trade-off between primary peak current, converter frequency and primary inductance. The primary peak current helps determine switching losses, as does the switching frequency. The ratio of the primary inductance to peak current determines the core size.

Common frequencies used are 50 kHz (in EMC-susceptible environments) and 100 kHz.

The ringing frequency at first valley detection is determined by the formula:

$$f_{ring} = \frac{I}{2 \times \pi \times \sqrt{L_p \times C_p}} \quad (7)$$

where:

$L_p$  = inductance of the primary winding

$C_p$  = parasitic capacitance on drain node.

Note that the total primary capacitance is not only determined by the primary inductor but also by the switch, the snubber diode, and the capacitance of the rectifier diode divided by the primary-to-secondary turns ratio:

$$C_p = C_{lp} + C_{sw} + C_{D5} + \frac{I}{n} \times C_{D6} \quad (8)$$

where:

$C_{lp}$  = capacitance of primary coil

$C_{sw}$  =  $C_{OSS}$  (MOSFET) switch, plus capacitance of DRAIN pin of SL2103

$C_{D5}$  = capacitance of the snubber diode

$C_{D6}$  = capacitance of the rectifier diode.

The time between transformer demagnetization and the first valley of  $f_{ring}$  is  $\frac{1}{2}$  of the period of the ringing frequency.

An estimation for  $C_p$  is made in the following example, where  $L_p = 415 \mu\text{H}$ :

$$C_p = 20 + 70 + 10 + \frac{I}{1.2} \times 20 = 117 \text{ pF} \quad (9)$$

Using [Equation 7](#),  $f_{ring} = 722 \text{ kHz}$ . As a result, the time for the first valley, after the second stroke has ended, is calculated as follows:

$$\Delta T = \frac{I}{2 \times f_{ring}} = 0.6 \mu\text{s} \quad (10)$$

A nominal converter frequency of 100 kHz has a period ( $\delta 1T + \delta 2T$ ) of 10  $\mu\text{s}$ . This gives an actual total period (including time to first valley detect) of 10.6  $\mu\text{s}$ . So the actual converter frequency, and the oscillator frequency, will be 94.3 kHz ( $f_{conv} = f_{osc} = 94.3 \text{ kHz}$ ).

The oscillator frequency is determined by the values of two parallel components; a resistor (R9) and a capacitor (C7). The capacitor is rapidly charged to  $V_{RC(max)}$  (typically 2.5 V; see [Ref. 1](#)) and discharged via the resistor to  $V_{RC(min)}$  (typical 75 mV; see [Ref. 1](#)). The discharge time has been calculated at  $3.5 \times RC$  seconds (RC being the oscillator time constant). The oscillator time constant for this example can be calculated using [Equation 11](#):

$$RC = \frac{I}{3.5} \times \left( \frac{I}{f_{osc}} - t_{RC(ch)} \right) \quad (11)$$

The oscillator charge time is derived from the SSL2103 specification ( $t_{ch(RC)} = 1 \mu\text{s}$ ; see [Ref. 1](#)). The values for both R9 and C7 can now be easily extracted from the RC time constant.

It is not recommended to use an oscillator capacitor of less than 220 pF as the drain voltage might distort the oscillator voltage. With a view to efficiency, a value for C7 of less than 1 nF is preferred.

Using [Equation 11](#), a switching frequency of 94.3 kHz would require an oscillator time constant of 2.74  $\mu\text{s}$ . This time constant can be achieved by connecting a 4.0 k $\Omega$  resistor (R9) and a 680 pF capacitor (C7) in parallel.

Dimming can be implemented by lowering the oscillator frequency. The frequency reduction range is determined by the ratio of R8 to R9. It is recommended that R8 should not be greater than 220 k $\Omega$  due to timing tolerance issues.

In the example for a dimming range between 100 % and 5 %, the frequency range will be from 94.3 kHz down to 4.8 kHz (maximum dimming). Applying [Equation 11](#) with a switching frequency of 4.8 kHz, R8 will be 87 k $\Omega$ . The nearest standard value is 91 k $\Omega$ .

## 6.4 External power switch

The PWR\_DRV output pin of the SSL2103 is used to drive the external power switch M1, (see block 3 [Figure 9](#)). The specification of this PWR\_DRV output is given in data sheet SSL2103 (see [Ref. 1](#)), and is optimized to minimize EMI influences and to provide high switching efficiency. The SSL2103 is capable of driving large power switches, with  $R_{Dson}$  down to 0.1  $\Omega$  or  $C_{iss}$  up to 4 nF. This is to be able to apply higher power applications than those of SSL2101 and SSL2102. The source and drain from the external MOSFET must be connected to the corresponding pins of the SSL2103. To enable efficient power switching, all control features such as valley switching and built-in demagnetization detection are the same as for the SSL2101 and SSL2102. The same applies to all built-in protection measures via the SOURCE input pin such as over-current protection and short winding protection. The over-current activation level must be fixed by defining R7 together with the  $I_{primary}$  of the transformer.

To select the external power switch type, the primary peak current and converter frequency must first be determined with the help of [Equation 6](#) in [Section 6.3](#). By choosing a power switch with low  $R_{Dson}$ , there will be less resistive power losses but more switching power losses will occur due to a larger drain capacitor. The efficiency of higher switching frequencies can benefit from choosing a power switch with a higher  $R_{Dson}$ . Optimum efficiency is attained by selecting the type of power MOSFET based on the lowest sum of losses due to  $R_{Dson}$  (see [Equation 12](#)) and the losses due to the switching frequency (see [Equation 13](#)).

### Losses due to MOSFET $R_{Dson}$ :

$$P_{R_{Dson}} = 1/3 \times \delta \times (I_{primarypeak})^2 \times R_{Dson} \quad (12)$$

### Losses due to MOSFET switching:

$$P_{sw} = P_{(loss\ switch-on)}$$

$$P_{sw} = 1/2 \times C_p \times (V_{valley})^2 \times f_{conv} \quad (13)$$

$C_p$  = total parasitic capacitance on drain node.

$$V_{\delta 2T} = V_{buf} + n \times V_o$$

$n$  = transformer winding ratio

In addition to the capacitive losses, there are also losses incurred due to hard switching of the current (see 5.3 of [Ref. 4](#)). The data sheets of the IC and MOSFET specify the switching slope at which the FET closes. During this time, there is an overlap of the current and voltage which causes dissipation. The dissipation increases with the switching time. These losses are reduced by using valley detection at switch-on. They are still present at switch-off.

### 6.5 Snubber circuit design

The snubber circuit (block 3 in [Figure 9](#)) uses a combination of a blocking diode (D5) and a zener diode (D4). In the applied power range (see [Table 2](#)), this approach is more efficient (lower losses) than alternative designs.

**Table 2. Flyback converter operating modes**

Method	Power range	Efficiency (% losses)
RC snubber	$P_O < 3 \text{ W}$	20 %
RCD clamp	full range	15 %
Zener clamp	full range	10 %

The maximum clamping voltage can be calculated using [Equation 14](#):

$$V_{zener} = V_{DRAIN(max)} - V_{buff(max)} - 25 \tag{14}$$

where:

- $V_{zener}$  = Value of zener diode D4
- $V_{DRAIN(max)}$  = Take lowest value from the two following parameters:
  - a. maximum voltage of DRAIN pin SSL2103 (= 600 V see [Ref. 1](#))
  - b. maximum voltage of DRAIN pin of the external connected MOSFET

A small safety margin of 25 V is included.

In the following example, for a maximum buffer voltage of 384 V and a maximum drain voltage of 600 V (derived using [Equation 14](#)), a 200 V zener diode was selected for D4.

$$V_{zener} = 600 - 384 - 25 = 191 \text{ V} \tag{15}$$

## 6.6 V<sub>CC</sub> generation

A circuit, consisting of a capacitor, a rectifier diode, a peak current limiting resistor and a protection zener diode, is used to generate an external V<sub>CC</sub> supply for the IC (see block 5 in [Figure 9](#)). The choice of component values involves a delicate trade-off between power dissipation and operation.

The values are determined by the output voltage, the transformer auxiliary-to-secondary turns ratio, the V<sub>CC</sub> current and the lowest converter frequency. V<sub>CC</sub> should be between 10.75 V (V<sub>CC(startup)(max)</sub>) and 28 V and the current I<sub>VCC</sub> should be 2 mA (see [Ref. 1](#)). Note that for SSL2103, the output current drawn from the SB\_DRV pin must be added, with the result that I<sub>VCC</sub> can go to maximum 5 mA. The zener diode requires a value that ensures sufficient energy is stored in the buffering capacitor without exceeding V<sub>CC</sub>. A practical value would be 20 V at 500 mW. The current delivered to the VCC circuit, at the highest converter frequency, determines the maximum dissipation.

The auxiliary-to-secondary turns ratio can be calculated using [Equation 16](#):

$$m = \frac{N_a}{N_s} = \frac{V_{aux}}{V_{led} + V_{D6}} \quad (16)$$

where:

m = auxiliary-to-secondary turns ratio

N<sub>a</sub> = the number of turns in the auxiliary winding

N<sub>s</sub> = the number of turns in the secondary winding

V<sub>aux</sub> = the voltage generated across the auxiliary winding

V<sub>D6</sub> = the voltage across D6 when it is conducting (normally between 0.3 V and 0.8 V)

V<sub>led</sub> = the voltage across the LED chain

The value of R5 can be calculated using the following formula:

$$R5 = \delta 2 \times \frac{f_{min}}{f_{max}} \times \frac{\delta I_{min}}{\delta I_{nom}} \times \frac{(V_{CC(min)} - V_{D7})}{I_{VCC}} \quad (17)$$

where:

f<sub>min</sub> = the minimum converter frequency during dimming

f<sub>max</sub> = the maximum converter frequency during dimming

δ1<sub>min</sub> = the minimum primary stroke duty factor at deepest dimming

δ1<sub>nom</sub> = the nominal primary stroke duty factor

V<sub>CC(min)</sub> = the nominal minimum value for V<sub>CC</sub> (> V<sub>CC(startup)(max)</sub>) - see [Ref. 1](#)

I<sub>VCC</sub> = the minimum current to be delivered to the IC to ensure reliable operation

D7 should be selected to withstand the peak current and reverse voltage. The switching speed should be sufficient to operate at the converter working frequency.

The reverse voltage depends on the primary-to-auxiliary turns ratio, the maximum buffer voltage and the maximum V<sub>CC</sub> voltage (which is equal to the zener voltage of D8).

$$V_{revD7} = \left( \frac{N_a \times V_{buff(max)}}{N_p} \right) + V_{zener} + V_{osc} \quad (18)$$

The maximum current through D7 is limited and can be calculated at start-up by dividing  $V_{aux}$  by the value of R5.

Capacitor C6 should provide sufficient buffering at the lowest frequency. This can be approximated with a linear model:

$$C6 = \frac{I_{VCC}}{\Delta V_{CC} \times f_{min}} \quad (19)$$

Assuming a  $V_{CC}$  ripple voltage of 100 mV with  $I_{VCC}$  estimated at 2 mA and  $f_{min} = 4.8$  kHz, using [Equation 19](#), C6 can be calculated as follows:

$$C6 = \frac{0.002}{(0.1 \times 4800)} = 4.2 \mu F \quad (20)$$

## 6.7 Bleeder settings

The SSL2103 has extended options for bleeder configurations with respect to the SSL2101 and SSL2102. The bleeder drive outputs SB\_DRV and WB\_DRV, can be used to drive external bipolar transistors or MOSFETs to switch the bleeder resistors. This mode corresponds with the behavior of the SSL2101 and SSL2102 with internal bleeder switches. The bleeder resistors must be defined as given in application note [Ref. 3](#).

To improve accuracy and efficiency, it is possible for the SSL2103 to use the bleeder outputs to generate current sources as shown in [Figure 9](#).

### 6.7.1 Design approach for defining strong and weak bleeder currents

The strong bleeder is designed to provide sufficient load for the dimmer to reset the dimmer timer and provide latch current. Tests have shown that the resetting of the dimmer timing is related to a fixed charge transfer. A current source in the SSL2103, becomes active, via the SB\_DRV pin, when the voltage on the HVDET pin falls below  $V_{th(HVDET)}$ , which is typically 52 V ([Ref. 1](#)). The strong bleeder current can be defined with T1 and R10. The output parameters of the SB\_DRV pin must be taken into account (see [Ref. 1](#)) when defining R18. To allow the system to operate with the majority of field installed dimmers, the strong bleeder resistor R10 must be set to the value given in [Table 3](#).

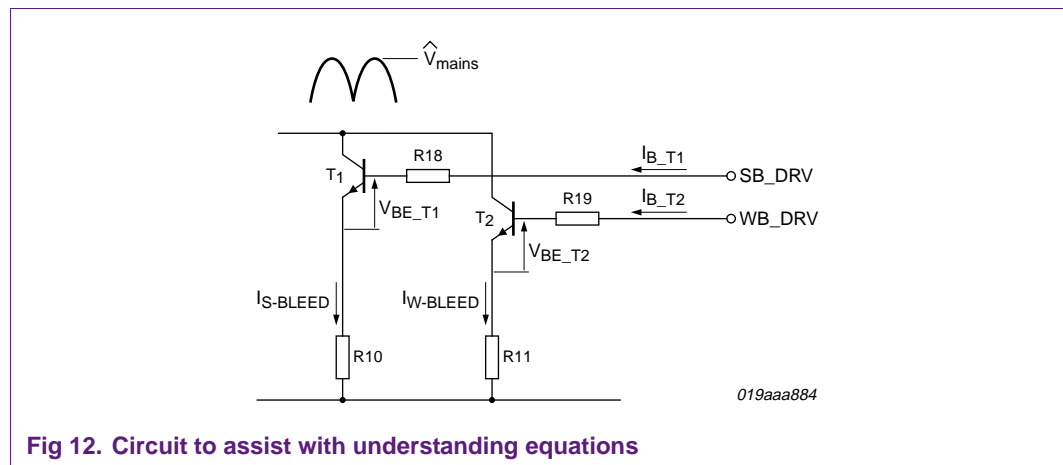
The weak bleeder is designed to maintain the hold current through the dimmer. It switches off when the voltage on the ISENSE pin drops below  $V_{th(low)ISENSE}$ , typically 250 mV. It switches on again when the voltage on the ISENSE pin rises above  $V_{th(high)ISENSE}$ , typically 100 mV (for both levels, see [Ref. 1](#)). Hysteresis is included to prevent unwanted oscillations. The weak bleeder current should switch on if the input current from the converter drops below the hold current of the dimmer. The weak bleeder current can be defined with R19, T2 and R11. The output parameters of the WB\_DRV pin must be taken into account when defining R19 (see [Ref. 1](#)). To allow the system to operate with the majority of field installed dimmers, the weak bleeder resistor R11 must be set to the value given in [Table 3](#).

Due to fact that current sources are used for bleeder operation, the resistor values provided in [Table 3](#) are not dependent on different mains voltages. However, the parameters for the bipolar transistor, such as maximum voltage and maximum power dissipation, must be reconsidered for different mains supply voltages (see [Table 3](#)). To optimize on efficiency, the resistor values provided in [Table 3](#), can be tuned to compensate for converter load.

**Table 3. Bleeder component settings**

Input voltage	R18	R10	R19	R11	Dissipation T1 (S-BLEED)	Dissipation T2 (W-BLEED) <sup>[1]</sup>
Universal	3.3 kΩ	0.13 kΩ	3.3 kΩ	1 kΩ	-	-
120 V (AC)	-	-	-	-	0.22 W	1.0 W
230 V (AC)	-	-	-	-	0.11 W	2.0 W
277 V (AC)	-	-	-	-	0.1 W	2.4 W

[1] These values are worst case figures for a maximum conduction time for T2.



**Fig 12. Circuit to assist with understanding equations**

To determine the required strong bleeder current, calculate the value of R10 as follows:

$$R10 = \frac{V_{SB\_DRV} - (I_{B\_T1} \times R18) - V_{BE\_T1}}{I_{required\ S-BLEED}} \tag{21}$$

$V_{SB\_DRV}$  can be found in [Ref. 1](#).

If  $I_{required\ S-BLEED} = 60\text{mA}$ , R10 must be approximately 0.13 kΩ.

The corresponding power dissipation of T1, can be calculated as follows:

$$P_{T1} = \frac{2I_{S-BLEED}}{\pi} (\hat{V}_{mains} (\cos\phi_1 - \cos\phi_2) - V_{E-T1} (\phi_2 - \phi_1)) \tag{22}$$

With:

$$\phi_1 = \arcsin\left(\frac{V_{E-T1}}{\hat{V}_{mains}}\right) \tag{23}$$

$$\varphi_2 = \arcsin\left(\frac{V_{th(HVDET)}}{\hat{V}_{mains}}\right) \quad (24)$$

$$V_{E\_T1} = V_{SB\_DRV} - I_{B\_T1} \times R18 - V_{BE\_T1} \quad (25)$$

$V_{th(HVDET)}$  can be found in [Ref. 1](#).

To determine the required weaker bleeder current, calculate the value of R11 as follows:

$$R11 = \frac{V_{WB\_DRV} - (I_{B\_T2} \times R19) - V_{BE\_T2}}{I_{required\ W-BLEED}} \quad (26)$$

$V_{WB\_DRV}$  can be found in [Ref. 1](#).

If  $I_{required\ W-BLEED} = 10\text{mA}$ , R11 must be approximately 1 kΩ. The corresponding power dissipation of T2 (when active), can be calculated as follows:

$$P_{T2} = \frac{2I_{W-BLEED}}{\pi} \left( \hat{V}_{mains} \cos\varphi_2 - V_{E\_T2} \left( \frac{\pi}{2} - \varphi_2 \right) \right) \quad (27)$$

With:

$$V_{E\_T2} = V_{WB\_DRV} - (I_{B\_T2} \times R19) - V_{BE\_T2} \quad (28)$$

$$\varphi_2 = \arcsin\left(\frac{V_{th(HVDET)}}{\hat{V}_{mains}}\right) \quad (29)$$

The ratio between R13 and R14 can be calculated using this data: Assume a dimmer requires a minimum hold current of 10 mA, which is maintained by means of the weak bleeder switch. Switch on at 10 mA over 200 Ω results in -2 V across R12 (or across R13 + R14). The weak bleeder switches on when the voltage on pin I<sub>SENSE</sub> (or across R14) is -100 mV. Therefore:

$$\begin{aligned} R14 / (R13 + R14) &= 100\text{ mV} / 2\text{ V} = 1 / 20 \Rightarrow \\ R13 + R14 &= 20 \times R14 \Rightarrow \\ R13 &= (20 - 1) R14 \Rightarrow \\ R13 / 19 &= R14. \end{aligned}$$

I<sub>SENSE</sub> is protected by R13 and should not exceed -5 mA. The maximum peak voltage is limited to 400 V by D2, but a safety margin of 100 V is applied. Therefore:

$$R13 = 500\text{ V} / 5\text{ mA} = 100\text{ k}\Omega.$$

$$\text{Therefore } R14 = 100\text{ k}\Omega / 19 = 5.3\text{ k}\Omega.$$

Note that all these resistors will need to be able to withstand peak power and peak voltage. T1 and T2 should be rated to withstand the voltage at which the TVS (D2) sets in and withstand the power dissipation. R12 should be rated to withstand the peak voltage and pulse energy at start-up. This pulse energy is listed in resistor data and can be calculated as follows:

$$E_{pulse} = 1/2 \times C_{3+4} \times V_{I(peak)}^2 \quad (30)$$



### 6.8 Dimming detection

The dimming reference voltage is derived from the non-buffered rectified mains voltage, and averaged using a capacitor. This voltage is input to the BRIGHTNESS and PWMLIMIT pins in the SSL2103 (see [Figure 9](#)). By balancing the voltage levels at these two inputs, the peak current through the inductor is reduced before the frequency of the converter falls. This eliminates audible noise from the transformer. The BRIGHTNESS and PWMLIMIT inputs have internal current sources, to which the working point of the converter is shifted. C8 provides filtering and has a recommended default value of 4.7 μF.

**Table 4. Recommended dimming circuit values**

Input voltage	R15	R16	R17
120 V (AC)	680 kΩ	15 kΩ	10 kΩ
230 V (AC)	1.5 MΩ	15 kΩ	10 kΩ
277 V (AC)	1.5 MΩ	15 kΩ	8.2 kΩ

R7 defines the dimming curve and regulates the maximum power delivered to the LEDs. It regulates the peak current through the inductor and thus the maximum power level. It also provides overcurrent protection to the converter. This technique removes part of the dependency between the output power and the mains voltage. The built-in overcurrent protection circuit triggers at 0.52 V. If the secondary losses and frequency are known, R7 can be calculated as follows:

$$R7 = \sqrt{\frac{f_{conv} \times L_p}{8 \times P_{in}}} \tag{31}$$

where  $P_{in} = P_{in(trans)}$  (see [Section 6.3](#)) + snubber losses.

### 6.9 Buffer circuit

The buffer circuit comprises two capacitors and an inductor. The circuit has dual functionality. The first function is to store energy to ensure the converter can transfer power continuously to the LED chain. LED operation becomes independent of dimmer operation and mains power fluctuations are filtered out. The second function is to filter ripple current generated by the converter to ensure compliance with legal requirements in relation to mains conducted emissions.

To implement the first function, the voltage across the converter should not fall below the minimum working voltage within a single mains cycle. The total capacitance (C3 + C4) can be estimated as follows.

Firstly, the minimum voltage at which the converter will still deliver full power needs to be calculated. It is either a duty-factor limit of 75% or the ratio of cycle time to cycle time minus secondary stroke time and it is derived from the calculated primary inductance and peak current:

$$V_{buff(min)} = \frac{I}{\partial_{lmax}} \times f_{conv} \times I_p \times L_p \tag{32}$$

Following this, the time between the peak voltage and when the mains voltage has reached this minimum voltage, needs to be calculated. Provide a margin of 10 V to allow for voltage drops during capacitor charging:

$$t_{dis} = \left(1 + \frac{2}{\pi} \times \arcsin\left(\frac{V_{buff(min)} + 10}{\hat{V}_{mains}}\right)\right) \times \frac{1}{4 \times f_{net}} \quad (33)$$

where  $f_{net}$  = frequency of the mains voltage:

$$\hat{V}_{mains} = V(AC)(RMS) \times \sqrt{2} \quad (34)$$

Now take the transformer input power and add IC losses and snubber losses. [Equation 35](#) can be used to calculate the total buffer capacitance:

$$C3 + C4 = \frac{2 \times P_{tot} \times t_{dis}}{\hat{V}_{mains}^2 - V_{buff(min)}^2} \quad (35)$$

where  $P_{tot} = P_{in} + IC$  losses.

The combination of L2, C3 and C4 constitutes a Pi-Filter that will help to filter out the high frequency currents generated by converter action. Although a single filter stage will not be enough to satisfy legal requirements in relation to mains conducted emissions, it will go a long way to achieve these goals. The cut-off frequency of this filter should be a magnitude below the converter frequency:

$$f_{cutoff} = \frac{1}{2 \times \pi \times \sqrt{L2 \times \frac{C3 \times C4}{C3 + C4}}} \quad (36)$$

Assuming  $C3 = C4$ . If the cut-off frequency is selected to be a decade below the working frequency, the resulting formula for L2 becomes:

$$L2 = \frac{100}{Cs \times 4\pi^2 \times f_{conv}^2} \quad (37)$$

where:  $Cs = C3 = C4$ .

It is recommended that a low-frequency absorbent soft ferrite material, such as 3S1 (Ferroxcube) or 3W1200 (Würth), be used for this inductor in order to dissipate high frequency energy and block unwanted oscillations.

## 6.10 Input circuit

The input circuit rectifies the mains voltage and provides overcurrent and overvoltage protection. It has to be over dimensioned to cope with overvoltage and overcurrent conditions on the input. Primary protection consists of a fuse or fusistor that breaks down when the current exceeds a specified value. If a fuse is used, a breakdown value should be selected that can handle inrush currents whilst still providing overcurrent protection. In practice, a value of between 1 A and 1.5 A is sufficient. If a fusistor is selected, the minimum value for this resistor can be calculated using [Equation 38](#). For most diode bridge rectifiers, the  $I_{FSM}$  parameter is around 20 A.

$$RI = \frac{\sqrt{2} \times V_{AC(max)}}{I_{FSM}} \quad (38)$$

Using [Equation 38](#), with 230 V (AC)  $\pm$  20 % and  $V_{AC(max)} = 276$  V, R1 is calculated as 19.5  $\Omega$  and the nearest E24 series standard value is 20  $\Omega$ .

In addition to its ohmic value, the continuous power dissipation in R1 is an important characteristic. This value can be determined using [Equation 39](#):

$$P_{R1} = C_{crestfactor} \times R1 \times \frac{P_{tot}^2}{V(AC)^2} \quad (39)$$

where the crest factor is the ratio of RMS to average current (typically 4).

With  $V(AC) = 230$  V,  $P_{tot} = 15.7$  W (see [Section 6.9](#)),  $R1 = 20$   $\Omega$  and crest factor = 4, the power dissipated in R1 will be 370 mW.

Capacitor C1 is added to improve differential mode filtering. By placing this component close to the mains input, the inductive coupling to mains is reduced. It also provides buffering against voltage spikes. The values of these input components are partly determined by the requirements of the dimmer. At low levels of output power, R4 can be added to reduce the audible noise generated by inrush current towards C3 and C4.

Components D1 and D3 should be dimensioned to handle the peak current in the circuit. The peak current is restricted by the combination of R12, R1 and R4.

$$I_{peak} = \frac{\sqrt{2} \times V_{(AC)(max)}}{R12 + R1 + R4} \quad (40)$$

At 230 V (AC)  $\pm$  20 %, if the values for  $R12 = 260$   $\Omega$ ,  $R1 = 20$   $\Omega$  and  $R4 = 0$   $\Omega$ , the peak current will be 1.4 A.

## 7. Transformer design parameters

One of the most challenging aspects of flyback design involves transformer calculations. A number of parameters affect the operation of the transformer some of which are, converter frequency, input/output voltage, input/output power, input peak current etc. In addition, a multitude of other factors, such as transformer size, material, core losses, proximity losses and ohmic losses, can be optimized to maximize transformer efficiency. To complicate matters further, there are a number of models available on which to base these calculations, with no consensus within the scientific community as to which model produces the best results. With so many variables to consider, and factors to trade off against one another, an optimal design can only be achieved through extensive prototype testing and measuring.

The SSL2103 can be used in flyback mode in applications to generate any power, due to the fact that the SSL2103 has a PWR\_DRV output to control an external power switch.

In addition to core size, careful consideration should be given to core geometry and core material. Core material should be selected for optimum (low) losses at the working temperature. For SSL2103 applications between 50 kHz and 200 kHz, the following core materials are recommended - 3C90 or 3F3 (Ferroxcube), N87 (Epcos) or TP4 (TDG).

For applications where cost is critical, e-cores are the most common choice. RM cores should be considered if shielding is critical.

**Table 5. Comparative geometry considerations for ferrite cores**

Aspect	Pot and RM core	Double stab core	E-core	Ec, ETD cores	PQ core	EP core	Toroid
core costs	high	high	low	medium	high	medium	very low
bobbin costs	low	low	low	medium	high	high	none
winding costs	low	low	low	low	low	low	high
winding flexibility	good	good	excellent	excellent	good	good	fair
assembly	simple	simple	simple	medium	simple	simple	none
mounting flexibility	good	good	good	fair	fair	good	poor
heat dissipation	poor	good	excellent	good	good	poor	good
shielding	excellent	good	poor	poor	fair	excellent	good

The application requires a transformer with three windings:

- a main or primary winding  $N_p$
- an output or secondary winding  $N_s$
- an auxiliary winding  $N_a$

The number of turns required must be calculated for each of the three windings.

### 7.1 Calculating the winding ratio

The following criterion must be met when selecting the winding ratio:

- the reflected output voltage should not exceed the zener snubber (D4) voltage
- $n_{(max)} = V_{zener} / V_{out}$

Example: if  $V_{zener} = 200\text{ V}$  and  $V_{out} = 35\text{ V}$  then  $n_{(max)} = 5.7$

The turn ratio is calculated with an empirical formula, and the result is limited by  $n_{(max)}$ :

$$n = 43.417 \times V_{out}^{-3/4}$$

Example: If  $V_{out} = 35\text{ V}$  then  $n = 3.01$ . Check to ensure that  $n < 5.7$ .

### 7.2 Calculating the primary inductance

The calculation of the primary inductance is performed using the following steps:

- **1 - Calculate  $\delta_1$  (duty cycle 1)**

The duty cycle at which the IC switch dissipation is acceptable needs to be calculated as follows:

$$\delta_1 = \frac{I - \frac{f_{conv}}{2 \times f_{ring}}}{I + \frac{V_{buffavr} \times I_{LED}}{P_{in} \times n}} \tag{41}$$

Example: If  $f_{conv} = 85\text{ kHz}$ ,  $f_{ring} = 303\text{ kHz}$ ,  $V_{buffavr} = (310+220) / 2 = 265\text{ V}$ ,  $I_{LED} = 350\text{ mA}$ ,  $P_{in} = 14\text{ W}$  and  $n = 3.01$ , then the value of  $\delta_1 = 26.8\%$ .

- **2 - Calculate  $\delta_2$**

$$\delta_2 = t_2 = \frac{I - \delta_1}{f_{conv}} - \frac{I}{2 \times f_{ring}} \tag{42}$$

Example: If  $f_{ring} = 303\text{ kHz}$ ,  $\delta_1 = 0.268$  and  $f_{conv} = 85\text{ kHz}$ ,  $t_2$  becomes  $7\text{ }\mu\text{S}$  resulting in  $\delta_2 = 59\%$ .

- **3 - Calculate the primary peak current ( $I_{p(peak)}$ ) and secondary peak current ( $I_{s(peak)}$ )**

$$I_{P(peak)} = \frac{\hat{I}_s}{n} \tag{43}$$

$$I_{s(peak)} = \frac{2 \times I_{LED}}{\delta_2} \tag{44}$$

Example:  $I_{LED} = 350\text{ mA}$ ,  $I_{s(peak)} = 0.7 / 0.59 = 1.186\text{ A}$ ,  $I_{p(peak)} = 0.394\text{ A}$ .

- 4 - Calculate the primary inductance

$$L_p = \frac{2 \times P_{in}}{I_{p(peak)}^2 \times f_{conv}} \quad (45)$$

Example: If  $P_{in} = 14 \text{ W}$  and  $f_{conv} = 85 \text{ kHz}$  then  $L_p = 2.1 \text{ mH}$ .

- 5 - Recalculate the ringing frequency

$$f_{ring} = \frac{1}{2 \times \pi \times \sqrt{L_p \times C_p}} \quad (46)$$

Example: If  $L_p = 2.1 \text{ mH}$  and  $C_p = 110 \text{ pF}$  then  $f_{ring} = 303 \text{ kHz}$

**Remark:** This is a circular calculation and steps 1 to 5 must be repeated for each new ringing frequency until the deviation from the previous calculation is minimal.

The ohmic loss in the switch can then be calculated as shown in [Equation 47](#):

$$P_{sw} = \frac{2 \times R_{DSon} \times P_{in(trans)}^2}{V_{buff(eff)}^2 \times \delta_1} \quad (47)$$

Example: With  $R_{DSon} = 6.5 \text{ } \Omega$ ,  $P_{in(trans)} = 14 \text{ W}$ ,  $\delta_1 = 26.5 \text{ } \%$  and  $V_{buff(eff)} = 289 \text{ V}$ ,  $P_{sw}$  will be  $115 \text{ mW}$ .

**Remark:** [Equation 47](#) not only dictates the primary inductance but also shows the relationship between primary current and power:

$$I_p = \frac{V_{buff} \times \delta_1}{L_p \times f_{conv}} = \sqrt{\frac{2 \times P_{input}}{L_p \times f_{conv}}} \quad (48)$$

Example: With  $V_{buff} = 265 \text{ V}$ ,  $P_{input} = 14 \text{ W}$ ,  $F_{conv} = 85 \text{ kHz}$ ,  $\delta_1 = 26.8 \text{ } \%$  and  $L_{prim} = 2.1 \text{ mH}$ , the value of  $I_p = 0.394 \text{ A}$ .

**Remark:** The initial calculation of primary duty factor was based upon minimizing the  $R_{DSon}$  switch losses. This formula is also used in the calculation tool. It might be beneficial to reduce primary duty factor thus creating higher IC losses but lower transformer losses and better output current stabilization/input voltage variation rejection. Assuming this will be applied to the limit, the minimum duty factor can be calculated using [Equation 49](#):

$$\delta_1 = \frac{2 \times R_{DSon} \times P_{in(trans)}^2}{V_{buff(eff)}^2 \times P_{sw(max)}} \quad (49)$$

Example: Assume  $P_{sw(max)}$  (allowable  $R_{DSon}$  switch losses) to be  $0.5 \text{ W}$  and  $V_{buff(eff)} = 265 \text{ V}$ , then  $\delta_1$  will become  $7.2 \text{ } \%$ .

A smaller  $\delta_1$  and larger winding ratio will lead to higher switch losses but has a number of advantages:

- It lowers primary inductance, thus reducing transformer size and losses
- In BCM, it makes the system less dependent on input voltage variation.

- In BCM, it makes the system react more to output voltage variation, which will lead to a more stable LED current.
- It allows a lower input voltage from which it still can deliver full power, thus bigger input voltage ripple and smaller input buffer capacitors.
- It allows for lower input voltage ripple providing the possibility to minimize input capacitance and increase output capacitance. This will give a high system power factor provided that the system stays in BCM mode.

**Remark:** It is advisable to select a primary duty factor that is between the formula as used to calculate minimum switch losses (which is also used in the calculation tool) and the above the formula that utilizes the allowed switch  $R_{DSon}$  losses.

### 7.3 Selecting the core type

The size of the core is determined by the maximum amount of energy to be stored in the transformer together with the required air gap. A core with a large air gap can store more energy in its air gap than a core with a small air gap. Also, the spread on the transformer's primary inductance ( $L_p$ ) will be lower for wide air gaps. The disadvantage of a wide air gap is the high leakage inductance of the transformer. A trade-off has to be made between storable energy, leakage inductance and tolerances on the inductance. The maximum energy that can be stored in the transformer can be calculated from [Equation 50](#) (see also [Equation 6](#)):

$$E = \frac{1}{2} \times L_p \times I_p^2 \tag{50}$$

The output power range determines which core types are suitable, as detailed in [Table 6](#):

**Table 6. Comparative geometry considerations for ferrite cores**

O/P power range	Core type	$A_e$ (mm <sup>2</sup> )
0 W - 2 W	E13/6/3	10.1
2 W - 4 W	E13/6/6	20.2
4 W - 6 W	E16/8/5	20.1
6 W - 11 W	E20/10/6	32.0
12 W - 14 W	E25/10/6	37.0
14 W - 25 W	E25/13/7	52.0

### 7.4 Primary winding count

There is a dependency between the air gap and the number of primary turns. The air gap must be big enough to avoid tolerance issues and small enough to minimize proximity losses (caused by the fringing field). In practice, an air gap of between 100 μm and 1 mm is advisable.

[Equation 51](#) and [Equation 52](#) can be used to establish a suitable balance between the air gap and the number of turns. The parameter  $A_e$  represents the effective core area in square meters (m<sup>2</sup>) and  $B_{max}$  represents the maximum flux density in Tesla. For most ferrite materials, a  $B_{max}$  value of 275 mT is low enough to prevent saturation. These values can be obtained from the core material data sheet.

The number of turns in the primary winding can be calculated using [Equation 51](#):

$$N_p = \frac{1}{22} \times \frac{\sqrt{L_p} \times I_p}{B_{max} \times A_e} \tag{51}$$

The air gap can now be calculated using empirical [Equation 52](#):

$$l_{gap(M)} = \frac{18 \times A_e}{\left( \frac{9 \times 10^6 \times L_p}{N_p^{1.9}} \right) - 50 \times \sqrt{A_e}} \tag{52}$$

### 7.5 Secondary winding count

To calculate secondary windings, take the number of primary windings and divide this by the winding ratio:

$$N_s = \frac{N_p}{n} \tag{53}$$

### 7.6 Auxiliary winding count

The number of windings for the transformer auxiliary output, depends on the output voltage of the converter. It can be calculated using [Equation 16](#) as stated in [Section 6.6](#)

### 7.7 Selecting wire diameters

Wire diameter selection involves a trade-off between size, ohmic losses, proximity losses and skin losses. For SSL2103 applications, skin losses are generally negligible for wire sizes below 0.6 mm in diameter at operating frequencies below 200 kHz. For wire diameters above 0.6 mm diameter, the use of Litze wire or multiple strands is recommended.

Ohmic losses are related to the peak currents in the wire. These can be estimated by obtaining the wire resistance, then calculating the average power dissipation. As a rule of thumb, the current density should be between 300 CM and 500 CM (Circular Mills per Amp). [Table 7](#) provides the appropriate wire sizes for a range of currents.

**Table 7. Wire selection table**

Diameter (mm)	Nearest AWG	Area (mm <sup>2</sup> )	Area (CM)	DC Res. OHM/M	Typical current level (Amp)
0.1	38	0.008	15	2.195	0.04
0.2	32	0.031	62	0.549	0.15
0.25	30	0.049	97	0.351	0.24
0.315	28	0.078	154	0.221	0.38
0.355	27	0.099	195	0.174	0.49
0.4	26	0.126	248	0.137	0.62
0.56	23	0.246	486	0.070	1.22
0.71	21	0.396	781	0.044	1.95



Table 7. Wire selection table ...continued

Diameter (mm)	Nearest AWG	Area (mm <sup>2</sup> )	Area (CM)	DC Res. OHM/M	Typical current level (Amp)
16 × 0.2	-	0.503	992	0.034	2.48
37 × 0.2	-	1.162	2294	0.015	5.73
61 × 0.2	-	1.916	3782	0.009	9.45

### 7.8 Proximity losses

For proximity losses, the calculations are too complicated to be discussed in this application note. What should be clear, however, is that they are closely related to the skin depth and the number of windings.

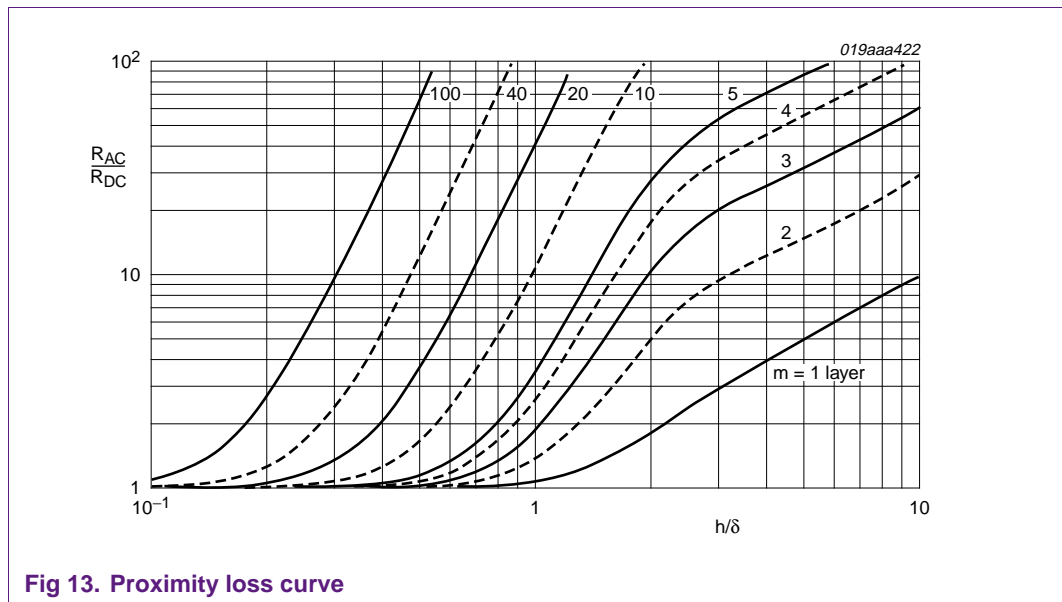


Fig 13. Proximity loss curve

The graph in [Figure 13](#) shows the ratio of AC-to-DC resistance for a section of a strip winding at different frequencies.  $\delta$  represents skin depth and  $h$  is the height of a square conductor. It can be seen that increasing the number of layers dramatically increases the resistance at high frequencies. For the SSL2103 operating between 50 kHz and 200 kHz using copper wire, the skin depth should be between 0.3 mm to 0.15 mm. Since the  $h / \delta$  ratio increases at higher currents, the number of winding layers should be minimized, even if it means selecting a higher current density.

## 8. Mains dimmer compatibility

### 8.1 Compatibility list

If the default values for the strong and weak bleeder resistors (R10 and R11) detailed in [Table 3](#) are used, the majority of existing wall mounted dimmers will be supported. The dimmers listed in [Table 8](#) have all been successfully evaluated.

**Table 8. Dimmer list**

Manufacturer	Type	Voltage (AC)	Power range	Load	Fuse
Opus	852.390	230	60-400	Ha/Inc	F1.6
Opus	852.392	230	20-500	Inc	T2
Bush-Jaeger	2250U	230	20-600	Ha/Inc	T3.15
Bush-Jaeger	2247U	230	20-500	Ha/Inc	T3.15
Bush-Jaeger	6519U	230	40-550	Ha/Inc	-
Gira	1184	230	60-400	Inc	T1.6
Everflourish	EFO700D	230	50-300	Ha/Inc	T1.25
Ehmann	10 UP-kpl	230	60-300	Ha/Inc	F1.25
Ehmann	39 Domus	230	20-500	Ha/Inc	T2A
Ehmann	4660	230	20-315	Ha/Inc	-
Lutron	TG-600PH-WH	120	600	Inc	-
Levitron	L12-6641-W	120	600	Inc	-
Levitron	L02-700-W	120	600	Inc	-
Levitron	6602-IW	120	600	Inc	-
Levitron	6683-W	120	600	Inc	-
Levitron	R12-6631-LW	120	600	Inc	-
Cooper	6001	120	600	-	-
Lutron	MIR-600THW-WH	120	600	Ha/Inc	-
Lutron	S-600PH-WH	120	600	Ha/Inc	-
GE	DI61-271	120	600	Inc	-
GE	DITC61-S71	120	600	Inc	-
GE	DIT61-71	120	600	Inc	-
GE	DIB61-71	120	600	Inc	-

The following problems may occur with some dimmers:

- At low dimming levels, a step function can be encountered in light output: the dimmer and converter interact and the dimmer output increases due to the increasing load.
- At certain dimming levels, the dimmer may react to an increase in load by reducing on time. This can lead to instability in the sensed voltage resulting in lamp flicker.

The effects of these problems can be minimized by weakening the relationship between the variable converter power and the load, as seen by the dimmer, either by increasing the load, or reducing the steepness of the dimming curve. This can be achieved by altering the values of R15 and R17. Note that the trade-off will be a reduced dimming range or an increase in power dissipation.

## 8.2 Transistor dimmers

A transistor dimmer may demand a higher load than can be realized with the standard bleeder values, to ensure the full voltage drop when dimming is turned off. Typically, a continuous load current of 10 mA or more is required.

The dimming range will be restricted with the standard dim-curve circuit, especially when deep dimming is combined with a low output load, because the average voltage drop will not be sufficient to detect dimming. To compensate for this, the dimming curve can be shifted but the trade-off will be a lower dim-range with triac dimmers. This will not be a problem as long as the output power is > 2.3 W in dimmed condition.

If the circuit needs to be compatible with both triac and transistor dimmers, and deep dimming is required at low output loads, an additional resistive bleeder can be connected in parallel with C1. A value of 22 kΩ / 3 W at 230 V (AC) or 12 kΩ / 1.5 W at 120 V (AC) would be appropriate.

A transistor dimmer with trailing edge operation doesn't need a hold current. Nor does it generate high inrush currents. These advantages over the standard triac dimmer can be exploited by omitting the damper network (R12/R13/R14). The ISENSE pin can be connected to GND. As a result, dissipation and audible noise will be reduced during dimming, and the inrush peak current will be reduced.

## 8.3 Multiple lamp circuits

The SSL2103 was designed to operate in a one-to-one situation - one lamp connected to one dimmer. However, it is possible to connect multiple lamps to a single dimmer. There is a restriction when using leading edge triac dimmers - the inrush current of all lamps must be combined if the dimmer is to withstand these inrush currents. Normal lamps and halogen lamps can generate inrush currents several times greater than the nominal current.

The inrush current can be calculated by, subtracting the buffer voltage across C3 and C4 (at maximum input voltage) from the input voltage and dividing this by the value of R12:

$$I_{inrush} = \frac{V_{in} - V_{buff}}{R12 + R1} \quad (54)$$

A standard value for this inrush current is 500 mA at 230 V (AC). This corresponds to a Halogen lamp of 50 W. When trailing edge dimmers are used, this inrush current is eliminated. The effective load of the lamp will be close to the nominal load.

## 9. Dimming curve calculations

The dimming curve describes the relationship between light output and the dimmer setting. The SSL2103 offers a great deal of freedom in dimming curve selection. The typical flyback application is an example of power steering: The output power, dissipated in the LEDs, is regulated by the IC. The current is determined by the forward voltage of the LEDs. The relationship between light output and the dimmer setting is defined in [Equation 55](#):

$$P = \eta \times I/2 \times L_p \times I_p^2 \times f \tag{55}$$

where  $\eta$  = estimated converter efficiency.

The SSL2103 has two control inputs: a BRIGHTNESS input that controls the output frequency and a PWMLIMIT pin that controls the on-time of the switch. If over-current protection is not enabled and/or the maximum duty factor of 75 % has not been exceeded, the LED power will correlate quadratically to the variation in duty factor. To enhance the performance of the system, a correction curve for the BRIGHTNESS pin voltage versus converter frequency was introduced. This correction curve compensates for the difference in light output between LEDs and incandescent/halogen lamps.

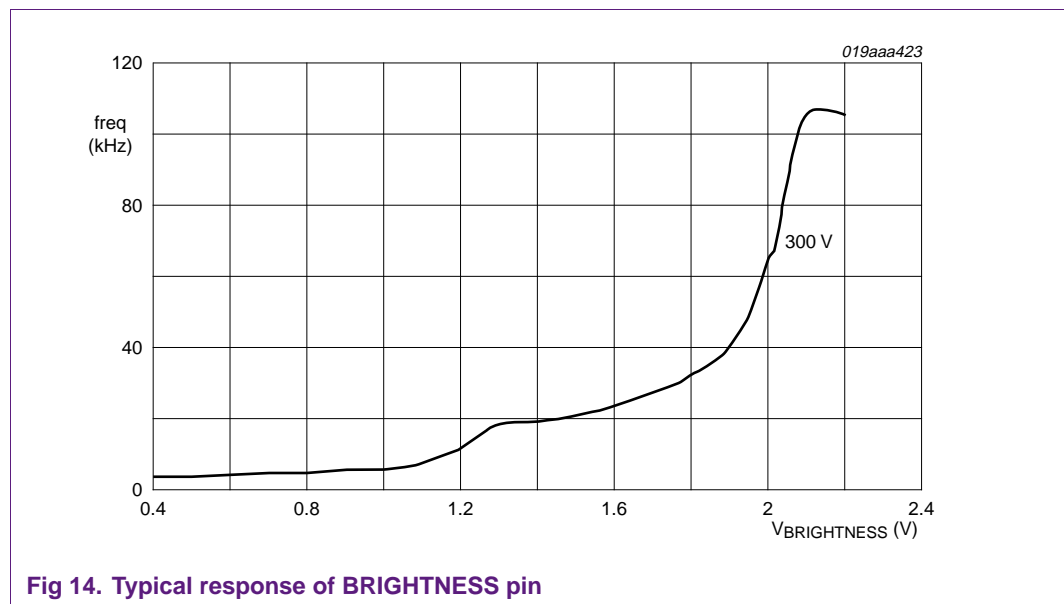


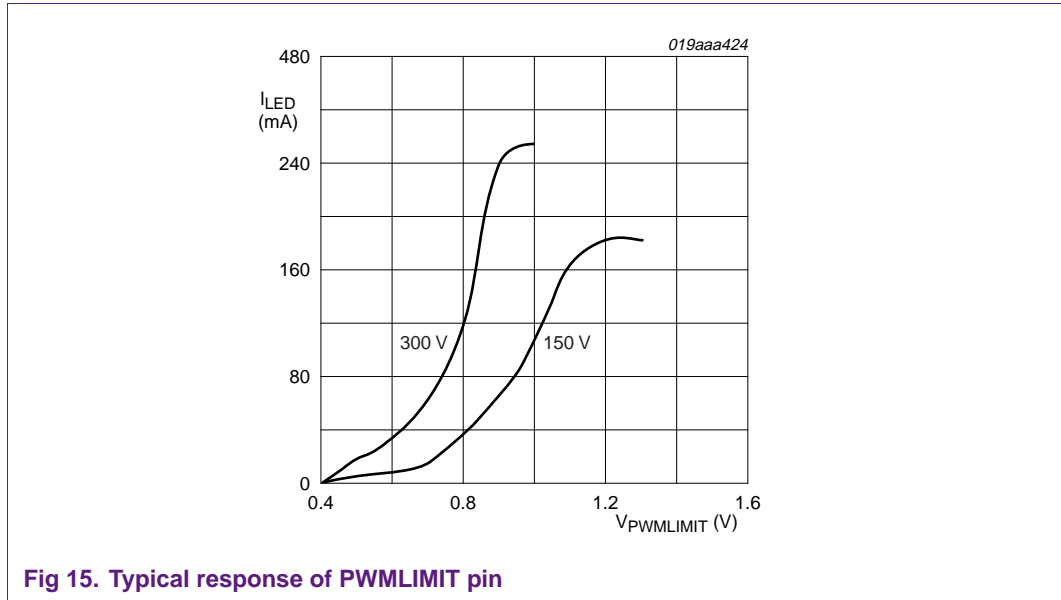
Fig 14. Typical response of BRIGHTNESS pin

As can be seen in [Figure 14](#), that the frequency of the converter varies between a minimum frequency determined by the values of C7 and R8, and a maximum frequency determined by C7 and R9. The frequency is independent of converter input voltage and load fluctuations.

Different rules apply to the PWMLIMIT input for which the peak current level varies with buffer voltage. The buffer voltage depends on the output load and dimmer setting and the resultant behavior is highly complex.

Although a dimming function can be implemented using only the PWMLIMIT input, when deep dimming is required, the brightness modulation is also used. The result enables a dimming range from 100 % down to 0.1 %. Resistor R16 is added to reduce audible noise.

The internal 20  $\mu\text{A}$  current source raises the voltage on the BRIGHTNESS pin. This shifts the brightness curve to the left, lowering the frequency at low dimmer settings. At these levels, the current controlled by the PWMLIMIT pin has already been reduced. The peak current through the inductor is the main source of audible transformer noise.



## 10. Summary

This document describes the construction of a flyback based converter which is a typical application for the SSL2103 mains dimmable LED driver. The differences of the SSL2103 with respect to the SSL2101 and SSL2102, are also discussed. It provides some general information concerning LED properties, some converter basics and mains dimmer aspects. The step-by-step design procedure provides the designer with information on how to dimension the components in this application and the functionality of the circuit. It contains a section on transformer design that should enable the designer to estimate values for the main transformer parameters such as core size, air gap, number of windings and wire size. It concludes with a description of mains dimmer dependencies and advice on solving potential dimmer problems.

## 11. Abbreviations

Table 9. Abbreviations

Acronym	Description
CM	Circular Mills
DC	Direct Current
EMC	Electromagnetic Compatibility
ESR	Equivalent Series Resistor
GND	Ground Potential
IC	Integrated Circuit
LED	Light Emitting Diode
MCM	Multi Chip Module
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
OCP	OverCurrent Protection
OTP	OverTemperature Protection
OVP	OverVoltage Protection
PWM	Pulse Width Modulation
RMS	Root Mean Square
SMPS	Switched-Mode Power Supply
SO	Small Outline
SSL	Solid State Lighting
SWP	Short Winding Protection
TLM	Temperature Lumen Management
V (AC)	Voltage Alternating Current

## 12. References

- [1] **Data sheet SSL2103** — SMPS controller IC for dimmable LED lighting.
- [2] **Data sheet SSL2101/SSL2102** — SMPS controller IC for dimmable LED lighting.
- [3] **AN10754** — SSL2101 and SSL2102 dimmable mains LED driver.
- [4] **AN10876** — Buck converter for SSL applications.

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